AN-ASXOXG-X Series Rev. -

U.S. Patent Number 7,812,682

Description

The Synchronized Crystal Oscillator is intended for use in the system, which requires multiple clocks in different nodes of the system to run synchronously in frequency **without master clock** along with SCC ensemble per 1138A. The Synchronized Crystal Oscillator is ideal for mission critical applications where optimization of system speed, bandwidth and redundancy is desired. SXO units are intended to be connected in the system as shown on Fig.1 to create a distributed oscillator. System nodes requiring synchronized clocks tap the signal off one of the synchronization buses, connecting individual SXO units.

Applications and Features

- Unlimited scalability/easily expandable
- Ideal for blade applications
- Provides a complete, system-wide clock redundancy solution
- High reliability systems with multiple synchronous clocks.
- Greatly improved system reliability due to redundancy and elimination of start-up problem
- Low Phase Noise and jitter
- No master clock, no PLL required for the system, no single point of failure
- No dynamic phase error
- Eliminates additive jitter degradation associated with clock distribution
- "Hot" – swappable
- Synchronize independent of power application sequence/No special power sequence required
- Improves Phase jitter at every node
- While in sync all units exhibit identical phase noise characteristics
- Low cost
- COTS/Dual use

NEL FREQUENCY CONTROLS, INC.

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Creating a Part Number

AN - A SXO X G - X

Package code
AN 8 pad 17x14 SMD

Operating Voltage
A 3.3 V ± 5%

Temperature Range, ºC
A 0 to 50
B 0 to 70
C -20 to 70
D -40 to 85
9 Customer Specific

Frequency Stability, Overall, ppm
G ±50

Environmental
L Contains a level of lead that is in excess of RoHS directive and is not designed for reflow
R RoHS compliant

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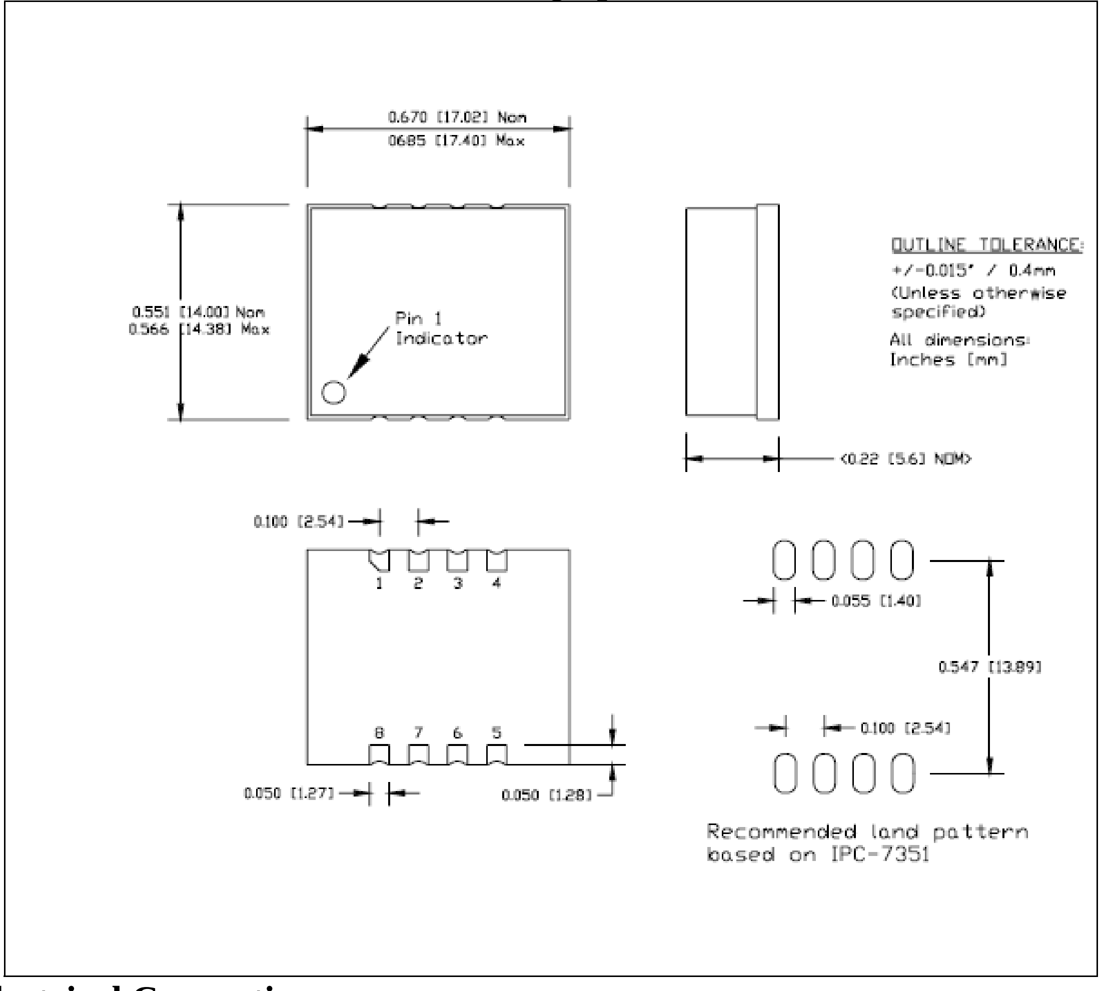
Drawing Specification



Electrical Connections

Pin out	#1 = Vcc (3.3V +/- 5%); #2 = Synch IN; #3 = Synch OUT; #4 = GND, Case; #5 = N/C, #6 = Contr OUT – DNC; #7 = GND, #8 = N/C

Environmental and Mechanical Characteristics

Operating temp. Range	see part # table
Mechanical Shock	Per MIL-STD-202, Method 213, Cond. A
Thermal Shock	Per MIL-STD-883, Method 1011, Cond. A
Vibration	Per MIL-STD-883, Method 2007, Cond. A
Hermetic Seal	Leak rate less than $1x10^{-8}$ atm.cc/s of helium , crystal only.
Soldering conditions	See MAX reflow profile below

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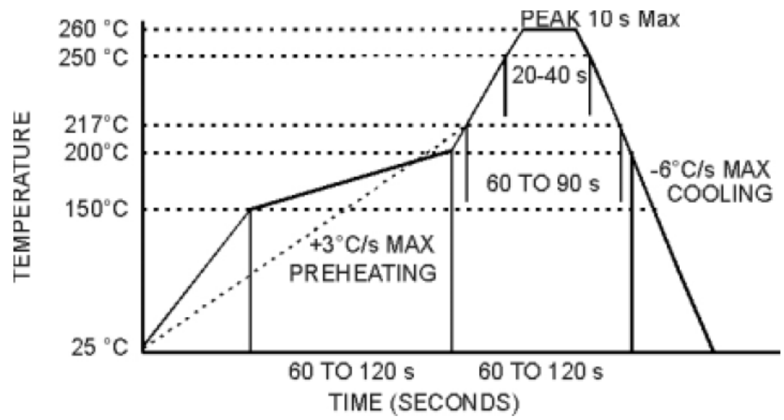
MAX Reflow Profile



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Operating Temperature Range	To	-40 to +85	ºC
Storage Temperature Range	Tst	-50 to +90	ºC
Supply Voltage	Vcc	-0.5 to 3.6	V
Sync in	Pk-to-pk	Vcc	V

Electrical Parameters (4)

Parameter		Symb	Conditions, Note		MIN	TYP	MAX	Unit
Nominal Frequency,		Fo			25		160	MHz
Supply Voltage		Vcc			3.135	3.3	3.465	V
Supply current		Icc	F = 100 MHz			20	30	mA
TEST OUTPUT(CMOS)	Load					15 pF/10 KOhm		
	Output Levels	Voh			0.7 Vcc			V
		Vol					0.1 Vcc	V
	Duty Cycle (Symmetry)		At 50% swing		45/55	50/50	55/45	%
	Rise/Fall Time	Tr/Tf	20 to 80, 80 to 20 %			3.0	5.0	ns
Jitter, test output see note 3	Integrated	J	Integrated from Phase Noise, 12 KHz to 20 MHz , RMS			0.1	0.2	ps
			10Hz to 80KHz,RMS				0.5	ps
			50 KHz to 80 MHz			0.3		ps
Sub-harmonics						none		dBc
Phase Noise		£(Δf)	100 MHz, test output	@ 10 Hz		-80		dBc/Hz
				@100 Hz		-110		
				@1 KHz		-135		
				@10KHz		-155		
				@100KHz		-160		
				@>1MHz		-160		

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Frequency Stability, individual unit, see note 3.	ΔF/F	Overall Initial Calibration Over temp 0 to 70 ºC -40 to 85 ºC Aging, 1st year 15 years Load, Vcc, shock, Vibration, reflow		±30 ±5 ±10 ±15 ±1 ±5 ±5	±35	ppm
Frequency Stability in ensemble, up to 100 units	ΔF/F	Overall			±40	ppm
Synchronization Range, individual unit	ΔF/F	Vsync in > 1.5 V pk-pk	±40			ppm
Number of SXO per system			2			See note 1.
Settling Time, "hot-swap", or powered up, powered down	Ts	After Vcc reaches 0.9 Vcc nom to plugged-in unit		10	50	ms
Sync out delay	Td			1		s

Notes

1. Consult Factory
2. Though it appears that there's very little margin of Sync range vs. Overall stability, following considerations should be taken into account
   a. The temperature difference in the same system between the nodes is much smaller than operating temperature range, assumed not to be greater than 10ºC
   b. Frequency drift of different units caused by aging, Vcc variations and reflow goes in the same direction

   Therefore in real life the margin will increase by 10 – 15 ppm.
3. Specified phase noise and jitter is for individual units tested separately. Using an ensemble of synchronized clock modules can produce system level phase noise and jitter performance akin to individual unit specified performance. This assumes that appropriate synchronization ensemble layout, isolation, and power supply filter techniques were used.
4. All parameters, unless otherwise specified, are at nominal conditions, ie: T=25°C, Nominal Vcc & Nominal Load.

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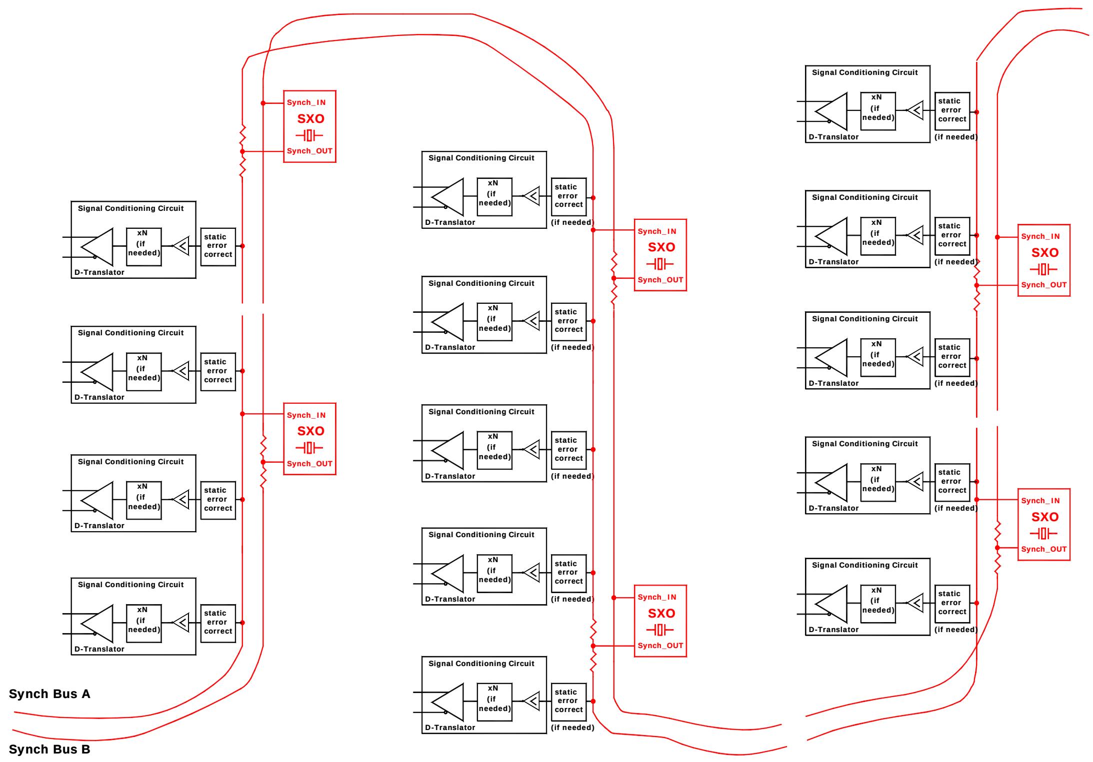

Fig. 1. Example of SXO connection in the system.

Explanation notes:

- Depicted ensemble in red should be considered as a giant **distributed** crystal oscillator.
- Individual SXO units are spread throughout the system roughly equidistantly physically.
- All SXOs are connected to the Sync Bus A and Sync Bus B in alternating fashion. Both buses are terminated at the ends. (Loop connection to be investigated)
- The role of the resistors at the SXO Synch OUT terminal is impedance matching
- The system nodes needed Synchronized clocking are fed from one of the buses (if phase synchronization and skew is not important both buses could be used)
- The synchronized clock is tapped off from any point on the bus. If Static phase error is needed to be corrected it runs through correction circuit (delay) into signal conditioning circuit. The number of system nodes can be much greater than the number of SXO units. As long as SXOs are spread equidistantly and within few inches from each other– the number of tap-offs can be as large as practical and not necessarily equal.

- Signal conditioning circuit consists of amplifier, frequency multiplier (if system clock frequency is higher than practical for the bus frequency), and logic translator (whatever logic system is using – bus is running essentially clipped sine-wave). Most likely differential translator.
- At that point the clock can be fed directly into a system node, or fan buffered if required.
- Synchronicity:
- All points on the bus are synchronous in frequency and don't have any noticeable dynamic phase error.
- Static phase error (which is constant for each node) can be corrected if needed. Skew will be very minimal and determined by the skew of fan-out buffer if used
- Redundancy, reliability: Failure of any arbitrary number of individual SXO cannot lead to the system failure. All remaining units will stay synchronous and provide signal on the buses to be tapped off by the system. Of course – no master clock – no single point of failure. No oscillator start-up problem – any with potential problem will get a jump-start from the bus Synch-in signal.
- Signal integrity/Noise: Signal on the bus gets cleaned up by the recursive filtering of each SXO unit. Phase noise (and jitter) on the bus signal is as good as the best SXO in ensemble.